

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Subhas Bothra, et al.	:	
Appl. No	:	09/523,403	:	Grp./Art Unit : 1775
Filed	:	March 10, 2000	:	Examiner: S. Stein
Title	:	Method of Using Films Having	:	
		Optimized Optical Properties for	:	
		Chemical Mechanical Polishing	:	
		Endpoint Detection	:	
			:	
Docket No.	:	PHA 51101A (New)	:	
		VLSI-3211.DIV (Previous)	:	

Assistant Commissioner for Patents
Washington DC 20231

RESPONSE and AMENDMENT

Sir:

This is in response to the Office Action of 12 December 2002.

IN THE CLAIMS

Please amend Claim 40 as follows.

- 1 40. (Amended) A structure, comprising:
- 2 a light transmissive dielectric layer having a planar surface portion
- 3 disposed above, and substantially vertically aligned with, an underlying reflective
- 4 patterned conductive line, the light transmissive dielectric layer further having a
- 5 non-planar portion, and a non-planar non-light-transmissive region disposed on
- 6 the non-planar portion of the light transmissive dielectric layer.

REMARKS

This is in response to the Office Action of 12 December 2002. Claims 32-43 are pending in the application, and all the pending Claims 32-43, have been rejected.

Claim 40 has been amended.

No new matter has been added.

In view of the amendments above and remarks below, Applicant respectfully requests reconsideration and further examination.

About The Invention

The present invention relates generally to structures suitable for use in integrated circuits, and more particularly relates to structures that facilitate end point detection during chemical-mechanical polishing. Various embodiments of the present invention include a dielectric structure having a non-planar layer of anti-reflective material embedded therein, wherein there are openings (i.e., windows or gaps), in the embedded anti-reflective layer such that at least a portion of the light, which is incident upon planarized surface areas of the dielectric structure corresponding to the regions of the openings, may be reflected back from underlying structures, and out through those openings.

Rejections under 35 USC 112, first paragraph

Claims 32-43 have been rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The Examiner states the term "conductive line" is not disclosed or defined in applicants' specification or claims, and that consequently, one of ordinary skill in the art can not make use of the claimed invention.

Applicants respectfully traverse the rejections under 35 USC 112, first paragraph, and request that they be withdrawn.

For at least the reasons set forth below, Applicants respectfully submit that the language "conductive line" is supported by the application as originally filed.

Applicants further submit that one of ordinary skill in the field of integrated circuit structures would readily comprehend Applicant's disclosure and the Claimed invention; and be in a position to make use of the Claimed invention.

With respect to the structure defined by the Claims, Applicants respectfully assert that this structure is very clearly shown in Fig. 6B. More particularly, Fig. 6B shows a planarized substrate 614; a planarized dielectric layer 616 disposed over substrate 614 and component 612; components 608 and 610 disposed on dielectric 616; a dielectric layer 606 disposed over components 608, 610, and dielectric 616, dielectric layer 606 having planar and non-planar surface portions; the planar surface portions being in substantial vertical alignment with components 608, 610; a non-planar reflectance stop layer 602 disposed over the non-planar portion of dielectric layer 606; and a planarized dielectric layer 604 disposed over non-planar reflectance stop layer 602.

With respect to the Examiner's contention that components 608, 610, can not be understood to be "conductive lines" within the teachings of Applicant's disclosure, the following is respectfully called to the Examiner's attention. In Applicants' previous amendment, wherein Claims 32-43 were added, it was noted that "[s]upport for these structures can generally be found throughout the specification; and can more particularly be found in the specification at page 21, line 21, through page 23, line 11, and in Fig. 6B." Consistent with these previously filed remarks, Applicants respectfully call the Examiner's attention to the specification at page 2, lines 1-3, where it is stated: "[c]omplex ICs can often have many different built up layers, each layer having components, each layer having differing interconnections, and each layer stacked on top of the previous layer." It is very well known in this field that "interconnections" are conductive lines that carry signals or power from one location to another within the integrated circuit. In fact, Chung (US Patent 5,792,707), which the Examiner cites in the current Office Action, refers to such a linguistic equivalency between conductors and interconnections at col. 3, lines 36-38, wherein it is stated: "the raised portions 22 14 preferably comprise a conductor (interconnect) 14 covered by an insulating layer 22" [emphasis added]. The Examiner's attention is further

called to page 15, lines 4-17, where it is explained that metal components (i.e., conductive lines) are covered with an inter-metal dielectric layer which is then required to be planarized, typically by chemical mechanical polishing. It is noted that the cross-sectional views of these components, which are shown in Applicants' figures, are a very common way of illustrating and describing conductive lines in all of the literature related to integrated circuit structures, including patents, reference articles, and textbooks related to integrated circuits.

In view of at least the foregoing, Applicants respectfully submit that the term "conductive line" as it is used in the Claims, can be readily understood by any person of ordinary skill in the field of integrated circuit structures.

No Art-Based Rejections of Claims 32-39

Applicants note that no rejections of Claims 32-39 have been made in view of the art of record.

Rejections under 35 USC 102(b)

Claims 40-41, and 43, have been rejected under 35 USC 102(b) as being anticipated by Chung (US Patent 5,792,707).

Independent Claim 40 has been amended, consistent with the specification, to more clearly and specifically recite a structure in accordance with the present invention. Support for this amendment can be found in Fig. 6B, and the associated text of the specification describing Fig. 6B. More particularly, it is made clear the Claimed structure includes a dielectric layer having both planar and non-planar portions and that the planar, light-transmissive portions are vertically aligned with the underlying components (i.e., conductive lines) which are light reflective; and that a non-planar, non-light transmissive region is disposed on the non-planar portion of the light-transmissive dielectric.

The structure defined by amended Claim 40 does not appear to be disclosed or suggested by Chung. In view of the foregoing, it is respectfully submitted that the rejections under 35 USC 102(b) have been overcome.

Rejections under 35 USC 103(a)

Claim 42 has been rejected under 35 USC 103(a), as being obvious over Chung (US Patent 5,792,707) and further in view of Hause (US Patent 6,013,574).

Independent Claim 40 has been amended as described in detail above, and Claim 42 depends indirectly from amended Claim 40. In view of the amendments, it is respectfully submitted that the combination of Chung and Hause does not produce the structure defined by the amended Claims.

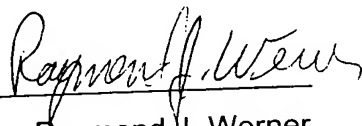
Conclusion

All of the rejections in the outstanding Office Action of 12 December 2002 have been responded to, and Applicants respectfully submit that the pending Claims 32-43 are now in condition for allowance.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By 
Raymond J. Werner
Reg. No. 34,752

Dated: 10 March 2003
Portland, Oregon

Version with markings to show changes made

In the Claims

- 1 40. (Amended) A structure, comprising:
- 2 a **light transmissive** dielectric layer having a **planar surface portion**
- 3 [light-transmissive region] disposed above, and substantially **vertically** aligned
- 4 with, an underlying **reflective** patterned conductive line, **the light transmissive**
- 5 **dielectric layer further having a non-planar portion,** and a **non-planar** non-
- 6 light-transmissive region **disposed on the non-planar portion of the light**
- 7 **transmissive dielectric layer** [surrounding the light-transmissive region].

Application No.: 09/523,403 Docket No.: PHA 51101A
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Attorneys: Zawilski/Werner Date Mailed: 10 March 2003

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